

WHAT IS CLAIMED IS:

3           1. A memory device comprising:  
4           a plurality of memory cells;  
5           a decoding circuit coupled to the plurality of  
6 memory cells, wherein the decoding circuit generate a first  
7 and a second control signal based on an address; and  
8           a power supply source coupled to selected ones of  
9 the plurality of memory cells based on the first control  
10 signal from the decoding circuit, wherein the power supply  
11 source provide one of a set of voltages based on the second  
12 control signal,  
13           wherein the selected memory cells are programmed  
14 in accordance with the voltage from the power supply source.

1           2. A memory device comprising:  
2           a plurality of memory cells;  
3           a decoding circuit to generate a set of control  
4 signals based on an address; and  
5           a plurality of bit lines that interconnect a  
6 subset of the plurality of memory cells,  
7           wherein the bit lines are implemented as floating  
8 bit lines.

1           3. An integrated circuit memory system  
2 comprising:  
3           a plurality of memory cells, each memory cell  
4 including a source, a drain, a control gate, and a floating  
5 gate, wherein the floating gate stores an electric charge,  
6 and wherein the memory cells are programmable by hot carrier  
7 injection; and  
8           a supply source for supplying voltages to the  
9 source, the drain, and the control gate of selected ones of  
10 the plurality of memory cells, and for controlling the  
11 current flowing between the source and drain during  
12 programming, said wherein program is controlled by the  
13 current flowing in the memory cells.